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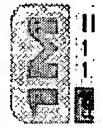
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1 [Drowsy caches: simple techniques for reducing leakage power](#)

Krisztián Flautner, Nam Sung Kim, Steve Martin, David Blaauw, Trevor Mudge

May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2

Full text available:

pdf(1.00 MB) [Publisher Site](#)



Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

On-chip caches represent a sizable fraction of the total power consumption of microprocessors. Although large caches can significantly improve performance, they have the potential to increase power consumption. As feature sizes shrink, the dominant component of this power loss will be leakage. However, during a fixed period of time the activity in a cache is only centered on a small subset of the lines. This behavior can be exploited to cut the leakage power of large caches by putting the cold c ...

2 [Physical interface: TAG: a Tiny AGgregation service for ad-hoc sensor networks](#)

Samuel Madden, Michael J. Franklin, Joseph M. Hellerstein, Wei Hong

December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI

Full text available:

pdf(2.19 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

We present the Tiny AGgregation (TAG) service for aggregation in low-power, distributed, wireless environments. TAG allows users to express simple, declarative queries and have them distributed and executed efficiently in networks of low-power, wireless sensors. We discuss various generic properties of aggregates, and show how those properties affect the performance of our in network approach. We include a performance study demonstrating the advantages of our approach over traditional centralize ...

3 [PACT 2001 workshops: Energy characterization of embedded real-time operating systems](#)

Andrea Acquaviva, Luca Benini, Bruno Riccò

December 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 5

Full text available:

pdf(484.99 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we propose a methodology to analyze the energy overhead due to the presence of an embedded operating system in a wearable device. Our objective is to determine the key parameters affecting the energy consumption of the RTOS allowing the development of more efficient OS-based power management policies. To achieve this

target, we propose a characterization strategy that stimulates the RTOS both at the kernel and at the I/O driver level by analyzing various OS-related parameters. Our ...

4 Energy Efficient Systems: Wake on wireless:: an event driven energy saving strategy for battery operated devices

Eugene Shih, Paramvir Bahl, Michael J. Sinclair

September 2002 **Proceedings of the 8th annual international conference on Mobile computing and networking**

Full text available:  pdf(798.63 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


The demand for an all-in-one phone with integrated personal information management and data access capabilities is beginning to accelerate. While personal digital assistants (PDAs) with built-in cellular, WiFi, and Voice-Over-IP technologies have the ability to serve these needs in a single package, the rate at which energy is consumed by PDA-based phones is very high. Thus, these devices can quickly drain their own batteries and become useless to their owner. In this paper, we introduce a techni ...

Keywords: low-power radio, power consumption of wireless LANs, wake-on-wireless

5 Virtual machines: Scale and performance in the Denali isolation kernel

Andrew Whitaker, Marianne Shaw, Steven D. Gribble

December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI

Full text available:  pdf(1.91 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

This paper describes the Denali isolation kernel, an operating system architecture that safely multiplexes a large number of untrusted Internet services on shared hardware. Denali's goal is to allow new Internet services to be "pushed" into third party infrastructure, relieving Internet service authors from the burden of acquiring and maintaining physical infrastructure. Our isolation kernel exposes a virtual machine abstraction, but unlike conventional virtual machine monitors, Denali does not ...

6 Session 2: Contents provider-assisted dynamic voltage scaling for low energy multimedia applications

Eui-Young Chung, Giovanni De Micheli, Luca Benini

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available:  pdf(253.91 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents a new concept of DVS (*Dynamic Voltage Scaling*) for multimedia applications. Many multimedia applications have a periodic property, but each period shows a large variation in terms of its execution time. Exact estimation of such variation is a crucial factor for low energy software execution with DVS technique. Previous DVS techniques focused only on end users (client sites) and their quality heavily depends on the accurateness of the worst case execution time estimatio ...

Keywords: DVS(Dynamic Voltage Scaling), characterization, contents provider, low-power, multimedia, worst case execution time

7 Managing Power Consumption in Networks on Chip

T. Simunic, S. Boyd

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  pdf(241.74 KB)

[Publisher Site](#)Additional Information: [full citation](#), [abstract](#)

Systems on a chip (SOCs) are rapidly evolving into larger networks on achip (NOCs). This work presents a new methodology for managing power consumption for NOCs. Power management problem is formulated using closed-loop control concepts, with the estimator tracking changes in the system parameters and recalculating the new power management policy accordingly. Dynamic voltage scaling and local power management are formulated in the node-centric manner, where each core has its local power manager that de ...

8 ECOSystem: managing energy as a first class operating system resource

Heng Zeng, Carla S. Ellis, Alvin R. Lebeck, Amin Vahdat

October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 37 , 30 , 36 Issue 10 , 5 , 5

Full text available: [pdf\(1.17 MB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Energy consumption has recently been widely recognized as a major challenge of computer systems design. This paper explores how to support energy as a first-class operating system resource. Energy, because of its global system nature, presents challenges beyond those of conventional resource management. To meet these challenges we propose the Currentcy Model that unifies energy accounting over diverse hardware components and enables fair allocation of available energy among applications. Our par ...

9 Task scheduling and real-time: System-level power-performance trade-offs in task scheduling for dynamically reconfigurable architectures

Juanjo Noguera, Rosa M. Badia

October 2003 **Proceedings of the 2003 international conference on Compilers, architectures and synthesis for embedded systems**

Full text available: [pdf\(451.82 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Dynamic scheduling for System-on-Chip (SoC) platforms has become an important field of research due to the emerging range of applications with dynamic behavior (e.g. MPEG-4). Dynamically reconfigurable architectures are an interesting solution for this type of applications. However, dynamic scheduling for run-time reconfigurable architectures with power-performance trade-offs has not been addressed in previous research efforts. In this paper, we address this open issue using a system-level approach ...

Keywords: clock-gating, dynamic scheduling, frequency scaling, power-performance trade-offs, reconfigurable computing

10 Work-in-progress session on innovative topics: SEAS: a system for early analysis of SoCs

Reinaldo A. Bergamaschi, Youngsoo Shin, Nagu Dhanwada, Subhrajit Bhattacharya, William E. Dougherty, Indira Nair, John Darringer, Sarala Paliwal

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: [pdf\(368.75 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Systems-on-chip (SoC) continue to be very complex to design and verify, despite extensive component reuse. Although reusable components are pre-designed and pre-verified, when they are assembled in an SoC there is no guarantee that the whole system will behave as expected from a performance, cost and integration point of view. In many cases this is because of faulty early design decisions regarding the architecture, core selection, floorplanning, etc. This paper presents a system for early analysis ...

Keywords: design analysis, design space exploration, floorplanning, performance, power

11 Energy efficient memory systems: Drowsy instruction caches: leakage power reduction using dynamic voltage scaling and cache sub-bank prediction

Nam Sung Kim, Krisztián Flautner, David Blaauw, Trevor Mudge

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**



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On-chip caches represent a sizeable fraction of the total power consumption of microprocessors. Although large caches can significantly improve performance, they have the potential to increase power consumption. As feature sizes shrink, the dominant component of this power loss will be leakage. In our previous work we have shown how the drowsy circuit---a simple, state-preserving, low-leakage circuit that relies on voltage scaling for leakage reduction---can be used to reduce the total energy co ...

12 Software-Only Bus Encoding Techniques for an Embedded System

Wei-Chung Cheng, Jian-Lin Liang, Massoud Pedram

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available:  pdf(174.60 KB)  Additional Information: [full citation](#), [abstract](#)
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Microprocessors with built-in Liquid Crystal Device (LCD) controllers and equipped with Flash memory are common in mobile computing applications. In the first part of the paper, a software-only encoding technique is proposed to reduce the power consumption of the processor-memory bus when displaying an image on the LCD. Based on the translation mechanism of the LCD controller, our approach is to start with the palette as a coding table for the pixel buffer and then reassign the codes according to ...

Keywords: memory bus encoding, low power, bus activity minimization, LCD, CompactFlash, Flash memory

13 Design space exploration and scheduling for embedded software: Leakage aware dynamic voltage scaling for real-time embedded systems

Ravindra Jejurikar, Cristiano Pereira, Rajesh Gupta

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available:  pdf(109.61 KB)  Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A five-fold increase in leakage current is predicted with each technology generation. While Dynamic Voltage Scaling (DVS) is known to reduce dynamic power consumption, it also causes increased leakage energy drain by lengthening the interval over which a computation is carried out. Therefore, for minimization of the total energy, one needs to determine an operating point, called the *critical speed*. We compute processor slowdown factors based on the critical speed for energy minimization. ...

Keywords: EDF scheduling, critical speed, leakage power, low power scheduling, procrastination, real-time systems

14 Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads

Steven M. Martin, Krisztian Flautner, Trevor Mudge, David Blaauw

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(189.46 KB)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Dynamic voltage scaling (DVS) reduces the power consumption of processors when peak performance is unnecessary. However, the achievable power savings by DVS alone is becoming limited as leakage power increases. In this paper, we show how the simultaneous use of adaptive body biasing (ABB) and DVS can be used to reduce power in high-performance processors. Analytical models of the leakage current, dynamic power, and frequency as functions of supply voltage and body bias are derived and verified w ...

15 Power awareness: A docked-aware storage architecture for mobile computing

Christopher R. LaRosa, Mark W. Bailey

April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available:  pdf(179.38 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We explore how the power-abundant docked state of mobile devices can be exploited to reduce power consumption during mobile operation and expand the capabilities of portable devices. We propose a storage hierarchy, which includes a hard disk, a large low-power cache, and a docked-aware file system that lowers the average power cost of file access from the disk while retaining the storage capacity of the disk. We investigate how hoarding files in low-power memory during a power-abundant docked st ...

Keywords: battery life, caching, docked, energy, file system, handheld, hoarding, palmtop, power

16 Special issue on wireless pan & sensor networks: A study of energy consumption and reliability in a multi-hop sensor network

Jonathan M. Reason, Jan M. Rabaey

January 2004 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 8 Issue 1

Full text available:  pdf(477.91 KB)

Additional Information: [full citation](#), [abstract](#), [references](#)

For a moderate-size, multi-hop, sensor network, we present experimental measurements of radio energy consumption and packet reliability. We categorize the energy measurements by energy consumed in each radio state and for each traffic type. Packet reliability results are presented from a network and link perspective, whereas prior work only considered the former. We introduce a novel technique of application-aware radio duty cycling called on-demand spatial TDMA. When compared to the non-cycling ...

17 Issues in data stream management

Lukasz Golab, M. Tamer Özsu

June 2003 **ACM SIGMOD Record**, Volume 32 Issue 2

Full text available:  pdf(195.61 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Traditional databases store sets of relatively static records with no pre-defined notion of time, unless timestamp attributes are explicitly added. While this model adequately represents commercial catalogues or repositories of personal information, many current and emerging applications require support for on-line analysis of rapidly changing data streams. Limitations of traditional DBMSs in supporting streaming applications have been recognized, prompting research to augment existing technolog ...

18 multithreaded context for robust conversational interfaces: Context-sensitive speech

recognition and interpretation of corrective fragments

Oliver Lemon, Alexander Gruenstein

September 2004 **ACM Transactions on Computer-Human Interaction (TOCHI)**, Volume 11
Issue 3

Full text available:  pdf(419.62 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We focus on the issue of robustness of conversational interfaces that are flexible enough to allow natural "multithreaded" conversational flow. Our main advance is to use context-sensitive speech recognition in a general way, with a representation of dialogue context that is rich and flexible enough to support conversation about multiple interleaved topics, as well as the interpretation of corrective fragments. We explain, by use of worked examples, the use of our "Conversational Intelligence Ar ...

Keywords: Context, corrections, dialogue, multithreading, recognition

19 Energy conservation for mobile devices: Sleep: a technique for reducing energy consumption in handheld devices

Lawrence S. Brakmo, Deborah A. Wallach, Marc A. Viredaz

June 2004 **Proceedings of the 2nd international conference on Mobile systems, applications, and services**

Full text available:  pdf(227.79 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Energy management has become one of the great challenges in portable computing. This is the result of the increasing energy requirements of modern portable devices without a corresponding increase in battery technology. *uSleep* is an energy reduction technique for handheld devices that is most effective when the handheld's processor is lightly loaded, such as when the user is reading a document or looking at a web page. When possible, rather than using the processor's idle mode, *uSleep* tri ...

Keywords: energy management, power management, processor sleep

20 Session 1: Standby power management for a 0.18µm microprocessor

Lawrence T. Clark, Neil Deutscher, Shay Demmons, Franco Ricci

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available:  pdf(227.57 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Static power dissipation is a concern for battery powered hand-held devices since it can substantially impact the battery life. Here, the use of reverse body bias to limit *I*off on the high performance, low power XScale™ microprocessor core is described. The scheme utilized is amenable to implementation on a low-cost (non-triple well) process and has limited regulation requirements. The regulation requirements and circuits are described, as is the performance of the method. A mea ...

Keywords: body effect, low power, microprocessors

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21 Energy efficient architectural techniques: Application adaptive energy efficient clustered architectures

Diana Marculescu

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: [pdf\(167.43 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As clock frequency and die area increase, achieving energy efficiency, while distributing a low skew, global clock signal becomes increasingly difficult. Challenges imposed by deep-submicron technologies can be alleviated by using a multiple voltage/multiple frequency island design style, or otherwise called, globally asynchronous, locally synchronous (GALS) design paradigm. This paper proposes a clustered architecture that enables application-adaptive energy efficiency through the use of dynamic voltage scaling.

Keywords: clustered architectures, dynamic voltage scaling

22 Scheduling techniques for embedded systems: Communication architecture based power management for battery efficient system design

Kanishka Lahiri, Sujit Dey, Anand Raghunathan

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: [pdf\(261.94 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Communication-based power management (CBPM) is a new battery-driven system-level power management methodology in which the system-level communication architecture regulates the execution of various system components, with the aim of improving battery efficiency, and hence, battery life. Unlike conventional power management policies (that attempt to efficiently shut down idle components), CBPM may delay the execution of selected system components even when they are active, in order to adapt the system to the available power.

Keywords: battery efficiency, communication architectures, embedded systems, low power design, power management

23 Cache and bus design: Dynamic power management for streaming data

Nathaniel Pettis, Le Cai, Yung-Hsiang Lu

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available:  pdf(129.01 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


This paper presents a method that uses data buffers to smoothen request variations and to create long idleness for power management. This method considers the power consumed by the buffers and assigns an energy penalty for buffer underflow. Our approach provides analytic formulas for calculating the optimal buffer sizes and the amount of data to store in the buffers. We use video prefetching as a case study and obtain power savings of more than 74% for MPEG-1 and 34% for MPEG-2 videos.

Keywords: dynamic power management, prefetching, quality of service, streaming video

24 Poster Session 2: An intra-task dynamic voltage scaling method for SoC design with hierarchical FSM and synchronous dataflow model

Sunghyun Lee, Kiyoun Choi, Sungjoo Yoo

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available:  pdf(190.32 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents a method of intra-task dynamic voltage scaling (DVS) for SoC design with hierarchical FSM and synchronous dataflow model (In short, HFSM-SDF model). To have an optimal intra-task DVS, exact execution paths need to be determined in compile time or runtime. In general programs, since determining exact execution paths in compile time or runtime is not possible, existing methods assume worst/average-case execution paths and take static voltage scaling approaches. In our work, we ...

Keywords: dynamic voltage scaling, finite state machine, formal model, low power, synchronous dataflow, variable supply voltage

25 Session S4.1: power in memory and network processors: An integrated approach to reducing power dissipation in memory hierarchies

Jayaprakash Pisharath, Alok Choudhary

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available:  pdf(295.32 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In recent years, both performance and power have become key factors in efficient memory design. In this paper, we propose a systematic approach to reduce the energy consumption of the entire memory hierarchy. We first evaluate an existing power-aware memory system where memory modules can exist in different power modes, and then propose on-chip memory module buffers, called Energy-Saver Buffers (ESB), which reside in-between the L2 cache and main memory. ESBs reduce the additional overhead incur ...

Keywords: RDRAM, dynamic cache, energy-delay product, energy-saver buffers (ESB), integrated approach, power

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mov*) <near/5> (power
<near/5>state)) <paragraph>
(buffer <or> fifo <or> queue)
```

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```
((chang* <or> switch* <or> mov*) <near/5> (power <ne
```

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L Number	Hits	Search Text	DB	Time stamp
1	1633	(711/154).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 16:37
2	413999	((chang\$3 or switch\$3 or mov\$3) near5 state) wiht ((buffer or FIFO) near10 monitor\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 16:38
3	91	((chang\$3 or switch\$3 or mov\$3) near5 state) with ((buffer or FIFO) near10 monitor\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 16:38
4	353	((711/154).CCLS.) and (((chang\$3 or switch\$3 or mov\$3) near5 state) wiht ((buffer or FIFO) near10 monitor\$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 16:38
5	2	((711/154).CCLS.) and (((chang\$3 or switch\$3 or mov\$3) near5 state) with ((buffer or FIFO) near10 monitor\$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 16:38
-	400290	(mov\$3 or chang\$3 or switch\$3) near5 state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:33
-	288	compar\$3 near10 ((buffer or FIFO) near3 level)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:36
-	58	((mov\$3 or chang\$3 or switch\$3) near5 state) and (compar\$3 near10 ((buffer or FIFO) near3 level))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:35
-	0	(compar\$3 near10 ((buffer or FIFO) near3 level)) with (power near5 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	684	(711/156).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	1415	(713/300).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	499	(713/340).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	551	(713/322).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	2065	(365/226).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:39
-	1	(compar\$3 near10 ((buffer or FIFO) near3 level)) and ((711/156).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:40

-	0	((compar\$3 near10 ((buffer or FIFO) near3 level)) and ((713/300).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:40
-	0	((compar\$3 near10 ((buffer or FIFO) near3 level)) and ((713/340).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:40
-	0	((compar\$3 near10 ((buffer or FIFO) near3 level)) and ((713/322).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:40
-	1	((compar\$3 near10 ((buffer or FIFO) near3 level)) and ((365/226).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:41
-	77	((compared near5 level) near10 ((chang\$3 or switch\$3 or mov\$3) near5 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 15:18
-	371	(710/56).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:45
-	381	(710/57).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:49
-	83	((mov\$3 or chang\$3 or switch\$3) near5 state) and ((710/57).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:49
-	57	((mov\$3 or chang\$3 or switch\$3) near5 state) and ((710/56).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 14:50
-	879	compar\$5 near10 ((buffer or FIFO) near5 level)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 15:19
-	42	((compar\$5 near10 ((buffer or FIFO) near5 level)) with state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 15:23
-	413257	((chang\$3 or switch\$3 or mov\$3) near5 state) wiht (buffer near10 monitor\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 15:24
-	91	((chang\$3 or switch\$3 or mov\$3) near5 state) with ((buffer or FIFO) near10 monitor\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 15:26